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James C. Scheller
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,473	TRIVEDI ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-69 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE, Amendment, and IDS as received on 8/12/2005.

Information Disclosure Statement

3. The examiner has not considered Scales III (U.S. Patent 6,334,176) listed on the 1492 filed by applicant on August 12, 2005, because the examiner has already cited these patents on the 892 attached the first Office Action mailed on December 14, 2004.

4. The examiner has not considered the foreign patent document and non-patent literature document because the information disclosure statement filed on August 12, 2005, fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the aforementioned documents have not been considered.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

6. Claims 18 and 51 are objected to because of the following informalities: Please replace "is" with --are--. Appropriate correction is required.

7. Claims 21, 31, 54, and 64 are objected to because of the following informalities: Please replace "two complement" with --two's complement--. Appropriate correction is required.

8. Claims 26 and 59 are objected to because of the following informalities: Please replace "string of bit" with --string of bits--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-2, 4-7, 9-20, 23-30, 32-35, 37-40, 42-53, 56-63, 65-66, and 68 are rejected under 35 U.S.C. 102(e) as being anticipated by Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari).

11. Referring to claims 1 and 34 Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

receiving a string of bits;

generating a plurality of indices using a plurality of segments of bits in the string of bits (Sazegari abstract, figures 3-4, column 2 lines 17-43, and column 4 lines 5-46);

looking up simultaneously a plurality of entries from a plurality of look-up tables using the plurality of indices. See Fig.4 and column 4, lines 24-32. Note that the table of Fig.4 is divided into two sub-tables (data1 and data2). Column 2, lines 17-26, further support this by saying that a table is logically divided into a number of smaller tables (i.e., multiple logical tables exist).

combining the plurality of entries into a first result (Sazegari abstract, figures 3-4, column 4 lines 5-67);

wherein the above operations are performed in response to the microprocessor receiving the single instruction (Sazegari column 4 lines 5-67, and figures 3-4), and note that the operations are performed in response to a single permute instruction.

12. Referring to claims 2 and 35 Sazegari has taught a method as in claim 1 further comprising:

receiving a plurality of data elements specifying the plurality of segments in the string of bits. See Fig.3, and note the string of bits 26. Each data element (byte field) specifies the segments. For instance, element 0 specifies that the first segment is 01. Element 1 specifies that the second segment is 14). Element 3 specifies that the third segment is 18. And so on.

13. Referring to claims 4 and 37 Sazegari has taught a method as in claim 3 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

14. Referring to claims 5 and 38 Sazegari has taught a method as in claim 2 further comprising:

receiving a bit pointer, wherein the plurality of segments in the string of bits are determined using the bit pointer and the plurality of data elements. See Fig.3, and column 4, lines 10-11. The bit pointer would be the address of the register used for providing the string of bits. The data elements (byte fields) of that register are then used to determine the segments by holding values corresponding to the segments. So, the register first must be located using a pointer, i.e., address (such as R2 or R5), and then each byte field (data element) of the register is read to determine the segments stored within.

15. Referring to claims 6 and 39 Sazegari has taught a method as in claim 5 further comprising:

generating a new bit pointer using the first result. See Fig.3, Fig.4, and column 4, lines 10-11. Note that when the first result is produced, it will be stored in a register (Fig.4, component 38). This register may later be used as a permute mask (Fig.3, component 26). When the new result is to be used as a mask for the permute instruction, a bit pointer must be generated to address the register holding the first result.

16. Referring to claims 7 and 40 Sazegari has taught a method as in claim 1 further comprising:

receiving an offset, wherein the plurality of indices are determined using the offset and the plurality of segments of bits. In order to determine the segments, the register holding the segments must be located. The register is located by supplying a register address (offset) in the permute instruction. A register address is an offset because it dictates the number of registers away the selected register is from register 0. For instance, if register 1 is to be selected as the permute mask, then register address 00001 (assuming 32 registers) would be provided. Address

00001, which corresponds to 1, indicates that the register to be selected (R1) is 1 register away from register 0 (R0). Likewise, if register 5 is to be selected as the permute mask, then register address 00101 (assuming 32 registers) would be provided. Address 00101, which corresponds to 5, indicates that the register to be selected (R5) is 5 registers away from register 0 (R0). The segments of the register 26 (Fig.3) are then used as indices into the lookup tables.

17. Referring to claims 9 and 42 Sazegari has taught a method as in claim 8 wherein the look-up memory comprises a plurality of look-up units, and wherein said partitioning look-up memory comprises:

configuring the plurality of look-up units into the plurality of look-up tables (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25).

18. Referring to claims 10 and 43 Sazegari has taught a method as in claim 23 wherein each of the plurality of look-up units comprises 256 8-bit entries (Sazegari column 3 lines 57-58, column 2 lines 35-43).

19. Referring to claims 11 and 44 Sazegari has taught a method as in claim 1 wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables. See column 4, lines 33-38. Note that if the table size is 32, then 5 bits are supplied in the instruction to address any one of the 32 entries. Since the instruction specifies a 5-bit value, and the 5-bit value specifies that there are 32 entries in the table, then it follows that the instruction specifies the total number of entries in the table. If applicant is suggesting that the size of the table is unknown prior to the instruction specifying an explicit size, then this concept should be claimed.

20. Referring to claims 12 and 45 Sazegari has taught a method as in claim 11 wherein the total number of entries is one of:

a) 256 (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25);

b) 512; and

c) 1024.

21. Referring to claims 13 and 46 Sazegari has taught a method as in claim 1 wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables. See Fig.3 and note that each permute instruction specifies that each entry uses 8 bits because the permute instruction indicates that 16 values are to be loaded into the result register (Fig.3). Since the result register is 128 bits wide, it follows that each value is 8-bits wide. So, the instruction indicates the bits used by each entry since the number of loads and the size of the register to be loaded are known.

22. Referring to claims 14 and 47 Sazegari has taught a method as in claim 13 wherein the total number of bits is one of:

a) 8 (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25);

b) 16; and

c) 24.

23. Referring to claims 15 and 48 Sazegari has taught a method as in claim 8 wherein the plurality of look-up tables are configured according to an indicator in an entry in a register file (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25).

24. Referring to claims 16 and 49 Sazegari has taught a method as in claim 15 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

25. Referring to claims 17 and 50 Sazegari has taught a method as in claim 1 wherein said combining the plurality of entries comprises:

selecting a valid data from the plurality of entries. See Fig.3 and Fig.4, and note that data is selected and combined into a single result. Entries that are read are assumed to be valid. Note that the selecting and combining occur in response to the permute instruction alone (in the case of Fig.4).

26. Referring to claims 18 and 51 Sazegari has taught a method as in claim 17 further comprising:

generating an indicator indicating whether none of the plurality of entries is valid. Entries that are not read are assumed to be invalid, i.e., they do not hold data that is required by the instruction. These entries are indicated by indicating the valid entries (if x+y=z, and you know x and z, then you also know y).

27. Referring to claims 19 and 52 Sazegari has taught a method as in claim 17 wherein the valid data is selected according to priorities of the look-up tables from which the plurality of entries are looked up. See Fig.3 and Fig.4 and note that more lookups need to be performed in data2. Therefore, it requires more attention and is given more attention than data1.

28. Referring to claims 20 and 53 Sazegari has taught a method as in claim 17 wherein said combining the plurality of entries further comprises:

formatting the valid data according to a type of the valid data. The valid data, when read, are stored into byte fields of the result register. The format is to have 16 bytes of data read and stored.

29. Referring to claims 23 and 56 Sazegari has taught a method as in claim 1 wherein an entry in the plurality of entries contains:

a) information indicating whether the entry is valid (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, which makes them valid).

b) information indicating a type of the entry; and

c) information indicating a number of bits of a code word to be decoded.

30. Referring to claims 24 and 57 Sazegari has taught a method as in claim 1 wherein the string is received from an entry in a register file (Sazegari Figure 3).

31. Referring to claims 25 and 58 Sazegari has taught a method as in claim 24 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

32. Referring to claims 26 and 59 Sazegari has taught a method as in claim 1 further comprising:

receiving a first number indicating a position of a last bit of input in the string of bit. The register address of the permute mask (Fig.3) would be such number since it indicates that the input string ends with the last bit in the selected register.

33. Referring to claims 27 and 60 Sazegari has taught a method as in claim 26 further comprising:

generating an indicator indicating whether any bit after the last bit of input is used in obtaining the first result. The signal to cause a write to occur to register 38 (Fig.4) is an indicator that bits encountered subsequent to the string of bits need to be written to the register in order to obtain the result.

34. Referring to claims 28 and 61 Sazegari has taught a method as in claim 12 further comprising:

generating an indicator indicating whether one of the plurality of segments of bits contains a predetermined code. The opcode for the instruction is an indicator that each segment will contain an 8-bit code used to index into lookup tables.

35. Referring to claims 29 and 62 Sazegari has taught a method as in claim 28 wherein the predetermined code represents an end of block condition. The opcode of the permute instruction indicates that the end of the input block occurs with the last amount of data in the register selected by the permute instruction as the permute mask.

36. Referring to claims 30 and 63 Sazegari has taught a method as in claim 1 further composing:

receiving at least one format;

formatting the string of bits into at least one escape data according to the at least one format; and

combining the at least one escape data and the first result into a second result. See Fig.3 and note that in addition to a permute mask 26, register operands (28, 30) are also be used. So, suppose that a permute instruction is executed, a table-memory lookup occurs and a first result is stored in register 28 (this would correspond to the operation shown in Fig.4 with the result being

stored in register 38). Then when a second permute instruction is executed, the string of bits in the permute mask are formatted into 16 groups of 8-bits (this is the format of the mask). Then, if one of the input registers 28 is the register in which the first result was stored, then the combination of mask and first result (and second operand register) would yield a second result 32.

37. Referring to claims 32 and 65 Sazegari has taught a method as in claim 30 wherein the at least one format is received from an entry of a register file (Sazegari abstract, figures 2-3, and 5, column 2 lines 17-43, column 3 lines 40-46, column 4 lines 5-46; column 2 lines 17-25).

38. Referring to claims 33 and 66 Sazegari has taught a method as in claim 32 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-3, and 5, column 2 lines 17-43, column 3 lines 40-46, column 4 lines 5-46; column 2 lines 17-25).

39. Referring to claim 68, Sazegari has taught a method as described in claim 1. Sazegari has further taught that each of the plurality of indices corresponds to a different one of the plurality of lookup tables. Dictionary.com defines a table as "an orderly arrangement of data, especially one in which the data are arranged in columns and rows in an essentially rectangular form." Consequently, looking at Fig.4 of Sazegari, memory 34, may be viewed as 1 table of 32 entries, 2 tables of 16 entries each, 4 tables of 8 entries each, and so on, until you have 32 tables of 1 entry each (1 row, 8 columns). Since there are 16 indices per permute instruction and 32 entries in the memory, they may each map to a different table if each of the indices is unique. For instance, if the memory is viewed as 32 tables (1 row/8 columns each), then they will all map to a different table provided the indices are unique. Or, if all the indices were odd numbers or all

even numbers, then they would each map to a different table among 16 tables (2 rows/8 columns each).

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. Claims 3, 8, 21-22, 31, 36, 41, 54-55, 64, and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sazegari, as applied above.

42. Referring to claims 3 and 36 Sazegari has taught a method as in claim 2 wherein the plurality of data elements are received from an entry in a register file. See Fig.3, component 26, and column 4, lines 10-11. Sazegari has further taught a media processor and a memory controller (if the system has memory (RAM), then it also has a memory controller, i.e., anything that controls/manages RAM in some way) but has not explicitly taught that they are integrated on a single integrated circuit. However, as shown in In re Larson 144 USPQ 347 (CCPA 1965), to make integral is generally not given patentable weight or would have been an obvious improvement. Integrated circuits allow for high speed communication between components since everything is on a single chip (additional/longer wires/buses connecting multiple chips are unnecessary). ICs also have low power dissipation and reduced manufacturing costs compared with board-level integration. As a result it would have been obvious to one of ordinary skill in

the art at the time of the invention to modify Sazegari such that the processor and memory controller are integrated.

43. Referring to claims 8 and 41 Sazegari has taught a method as in claim 1 further comprising:

a) partitioning look-up memory into the plurality of look-up tables before said looking-up (Sazegari column 2 lines 17-25);

b) Sazegari has not explicitly taught that the microprocessor is a media processor formed on a monolithic integrated circuit. However, Official Notice is taken that processors being formed on an integrated circuit is well known and expected in the art. ICs allow for low power dissipation and lower manufacturing costs. Furthermore, as shown in In re Larson 144 USPQ 347 (CCPA 1965), to make integral is generally not given patentable weight or would have been an obvious improvement. As a result it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sazegari such that the processor is formed on a monolithic integrated circuit.

44. Referring to claims 21 and 54 Sazegari has taught a method as in claim 20. Sazegari has not taught that the type of the valid data is one of:

a) zero fill;

b) sign magnitude; and

c) two complement.

However, Official Notice is taken that it is well known in the art to represent binary data in two's complement form. Such a form allows the system to efficiently represent negative

numbers as well as positive numbers. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sazegari to include two's complement data.

45. Referring to claims 22 and 55 Sazegari has taught a method as in claim 21. Sazegari has not taught retrieving a sign bit from the string of bits for the valid data, wherein the first result is obtained by formatting the valid data using the sign bit when the type of the valid data is sign magnitude. However, Official Notice is taken that sign magnitude notation is well known in the art. This format allows for straightforward way to represent positive and negative numbers. The format choice is really nothing more than a designer choice. Different designers choose different formats for different reasons. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sazegari to include a sign magnitude format, which would include the specifics set forth above.

46. Referring to claims 31 and 64 Sazegari has taught a method as in claim 30. Sazegari has not taught that the at least one format is for data of a type which is one of:

a) zero fill;

b) sign magnitude; and

c) two complement.

However, Official Notice is taken that it is well known in the art to represent binary data in two's complement form. Such a form allows the system to efficiently represent negative numbers as well as positive numbers. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sazegari to include two's complement data.

47. Referring to claim 69, Sazegari has taught a method as described in claim 1. Sazegari has not taught that each of the plurality of look-up tables is larger than a vector register. However, as

shown in In re Rose, 105 USPQ 237 (CCPA 1955)m changes in size/range are generally not given patentable weight or would have been obvious improvements. Clearly, the size of the lookup tables may be increased to hold more data. This would cause the amount of possible indices to grow and therefore, the instruction would also have to be modified to include less indices. But, the general idea still remains. Simultaneous lookups to multiple tables is still taught by Sazegari. Smaller tables may be used, bigger tables may be used, and other features may be adjusted to accommodate the changed sizes of the tables, but the process of simultaneously looking up still remains the same. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sazegari such that each of the lookup tables is larger than a vector register.

48. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sazegari, as applied above, in view of Shams, U.S. Patent No. 5,526,501.

49. Referring to claim 67, Sazegari has taught a method as described in claim 1. Sazegari has not taught that the plurality of segments of bits in the string of bits are of variable lengths. However, Shams has taught multiple lookup tables of varying size. See column 3, line 49, to column 4, line 9. Consequently, the segments that are used to index into the tables would also be of varying size. By having tables of varying size, more or less data may be stored in any given table. For processes which involve a lot of data of one type may store that data in a larger table whereas if it involves much less data of another type, the data may be stored in a smaller table, thereby leaving a bigger table for an application that needs it. In addition, the size of the tables are not critical when it comes to Sazegari. Sazegari merely teaches making simultaneous

lookups from multiple tables. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sazegari in view of Shams such that multiple tables of varying size are included, and consequently, multiple segments of varying size are included.

Response to Arguments

50. Applicant's arguments filed on August 12, 2005, have been fully considered but they are not persuasive.

51. Applicant argues the novelty/rejection of claim 1 on page 14 of the remarks, in substance that:

> "It is clear that Sazegari describes the simultaneous lookups in a single table. Sazegari does not suggest simultaneous in multiple sub-tables."

52. These arguments are not found persuasive for the following reasons:

a) See Fig.4 and column 4, lines 24-32. Note that the table of Fig.4 is divided into two sub-tables (data1 and data2). Column 2, lines 17-26, further support this by saying that a table is logically divided into a number of smaller tables (i.e., multiple logical tables exist).

53. Applicant's argument with respect to claims 2-3 and 5-7 are moot in view of the new grounds of rejection.

54. Applicant argues the novelty/rejection of claim 8 on page 17 of the remarks, in substance that:

> "Sazegari shows dividing a large table into a number of smaller tables. Sazegari does not show the partitioning of look-up memory."

55. These arguments are not found persuasive for the following reasons:

a) Fig.4 clearly shows that memory 34 is a lookup memory. Indices are applied to the memory via register 36, and data values are read from the indexed locations and written to an output register 38. And, as discussed, the memory is partitioned into smaller tables. Therefore, Sazegari has taught partitioning (dividing up) lookup memory.

56. Applicant's argument with respect to claims 11, 13, 17, 26, and 30 are moot in view of the new grounds of rejection.

Conclusion

57. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Li et al., U.S. Patent No. 5,619,516, has taught efficient CRC remainder coefficient generation and checking device and method in which an input is segmented into indices, the indices are used to index into multiple lookup tables, and the outputs of the tables are XORed (combined) together (Fig.4)

DesJardins et al., U.S. Patent No. 6,029,186, has taught high speed calculation of cyclical redundancy check sums in which a message is split into segments, the segments are modified via an addition operation, and then each index is used to index into a separate lookup table. The outputs of the tables are also combined (Fig.5).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
October 18, 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100